FABRICATING SEMICONDUCTOR CHIPS

Field of the Invention

The present invention relates generally to fabricating semiconductor chips, and, more particularly, to a method of preparing semiconductor chips for debugging and failure analysis.

Background of the Invention

In the fabrication of semiconductor chips, an important step is selectively etching and/or adding metal to selected portions of the completed chip in order to debug problem areas. Typically, this involves using a focused ion beam (FIB) system in the desired areas in order to remove and/or add selected connector portions. The desired areas are usually identified by the FIB system using topological features for imaging contrast and navigation to the regions of interest. The FIB systems can then add or remove features depending on the gas applied.

In some devices, however, the entire chip is covered by one or more planarization layers, thereby hiding the topographical features which are used for aligning the focused ion beam. In some cases, the only features resolvable by the FIB system are the bonding pads. However, since the accuracy desired for FIB is generally in the range 0.1 to 0.2 microns, the pads cannot be used for alignment.

It is desirable, therefore, to provide a process permitting navigation of a focused ion beam on an otherwise planar Integrated Circuit (IC) chip.

Summary of the Invention

To achieve these and other objects, and in view of its purposes, the present invention provides a method of fabricating a semiconductor chip which includes a passivation layer over the chip surface. At least two alignment marks are formed in or on the passivation layer. A focused ion beam can then be applied to a selected portion of the chip using the alignment marks to locate the selected area.

In accordance with another aspect, the invention is a semiconductor chip which includes a passivation layer as a top layer. At least two alignment marks are formed in or on the passivation layer to provide topological features for locating selected areas of the chip.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention.

Brief Description of the Drawing

The invention is best understood from the following detailed description when read in connection with the accompanying drawing. It is emphasized that, according to common practice in the semiconductor industry, the various features of the drawing are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Included in the drawing are the following figures:

Fig. 1 is a plan view of a semiconductor chip including alignment marks according to an embodiment of the invention;

Fig. 2 is a cross sectional enlarged view of a portion of the chip of Fig 1;

Fig 3 is a plan view illustrating the shapes of the alignment marks which may be used according to one embodiment of the invention;

Fig 4 is an enlarged plan view of a portion of the chip illustrated in Fig 1;

Fig 5 is a cross sectional view of a portion of a chip in accordance with another embodiment of the invention; and

Fig 6 is a cross sectional view of a portion of a chip in accordance with yet another embodiment of the invention

Detailed Description of the Invention

Referring now to the drawing, wherein like reference numerals refer to like elements throughout, Fig. 1 is a plan view of a typical semiconductor chip, 10, which includes features of the present invention in accordance with one embodiment, and Fig 2 is a cross sectional enlarged view of a portion of that chip taken along line 2-2 of Fig 1. The chip illustrated is essentially completed and includes bonding pads, e.g., 11, to which wire bonds (not shown) are bonded. The chip also includes the standard topological features such as alternate layers of dielectric and conductive layers, 20 of Fig 2, formed over the semiconductor substrate, 12. These features are hidden in the final chip due to the formation of one or more planarization layers, 13 and 21, formed over essentially the entire surface of the chip. In this example, the substrate, 12, was silicon, and the planarization layers, 13 and 21, were polyimide and silicon nitride formed by standard techniques such as plasma enhanced chemical vapor deposition. The chip also includes metal areas, e.g., 22, on the surface through which bonding pads, e.g., 18, provide electrical contact to the underlying conductive layers.

In order to provide alignment for the subsequent focused ion beam (FIB) etching and/or addition of metal portions, a plurality of alignment marks, 14-17 are formed on the top most planarization layer, 21. In this example, there are four marks, one each at one of the corners of the chip. However, other patterns are possible strewn all across the surface of the IC chip. As illustrated in Fig 3, the marks are essentially in the shape of a cross, but can include rectangular portions, or "hammer heads" at one or more ends of the cross. For example, the alignment mark, 14, located at the lower left corner of the chip includes rectangular portions 31-34 at each end of the cross. Mark 15 includes three rectangular portions, mark 16 includes two portions, and mark 17 includes only one such portion. The purpose of these portions is to indicate in which quadrant of the chip the mark lies. Other patterns for the marks are possible.

As illustrated in the enlarged view of Fig 4, the alignment marks, e.g., 14, can be formed so that one edge of each cross bar, e.g., 41 and 42, is aligned with an edge, 43 and 44, of a corresponding bonding pad, 18 and 19. This is done purely for the sake of convenience, and the marks can be formed anywhere on the passivation layer.

The marks in this example were formed by standard metal deposition techniques, e.g., sputter deposition, at the same time as the bond pads. The metal in this example was an aluminum copper alloy for both the pads and alignment marks. Again,

this is for convenience, and the marks need not be formed at the same time or with the same material as the bonding pads.

Before the marks are formed on the chip, their position relative to the center of the chip was recorded in the computer aided design (CAD) database. After the marks were formed on the chip, the CAD layout was superimposed over an image of the chip surface generated by the FIB system using the marks in the database and on the chip for alignment. Once this superposition is achieved, any component can be located on the chip even though hidden by the passivation layer. Preferably, four marks are used for accuracy. However, two or three marks can also be used.

Fig 5 illustrates a cross sectional view of a chip in accordance with another embodiment of the invention. This example is similar to the previously described embodiment except for the fact that the metal alignment marks, e.g., 14, are formed on the surface of the first passivation layer, 13, and the second passivation layer, 21 is then formed over the mark. If the passivation layer, 21, is sufficiently thin, typically one third to three quarters of the thickness of the metal alignment marks, the layer will form bumps, e.g., 50, which conform to the shape of the metal marks. Since the bumps have a height, d, above the surface of the top passivation layer, 21, topological features are formed which can be used in the subsequent FIB processing. Alternatively, as illustrated in Fig 6, the metal marks, 14-17 could be eliminated entirely, and the topological features formed by etching any desired pattern into the top passivation layer.

Subsequent to the formation of the alignments marks, a standard focused ion beam apparatus was used to locate and etch away or add selected areas of the hidden conductors. The apparatus acted as a standard scanning electron microscope which located the selected areas using the height difference between the marks and the passivation layer as reference points.

Thus, in accordance with the invention and in the attached claims, it should be understood that the term "alignment mark" can include any topological feature formed in or on the top passivation layer which can be used by a scanning electron microscope and/or FIB system to locate components on the chip.

Although the invention has been described with reference to exemplary embodiments, it is not limited to those embodiments. For example, although the

examples described above involved wire bonded chips, the invention could also be used in Flip-Chip bonded designs. Rather, the appended claims should be construed to include other variants and embodiments of the invention which may be made by those skilled in the art without departing from the true spirit and scope of the present invention.